Verification of dynamic systems with locks and variables

Corto Mascle
joint work with Anca Muscholl, Igor Walukiewicz

PaVeDys

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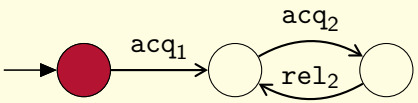
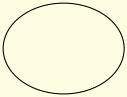
Lock-sharing systems[1]





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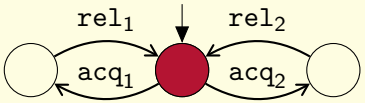

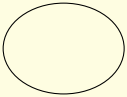

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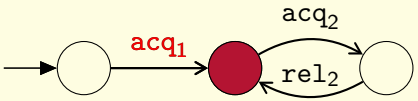

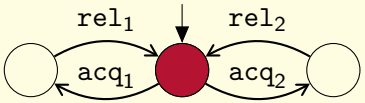

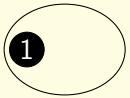

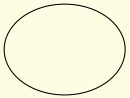

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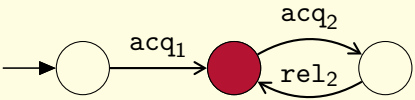

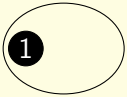

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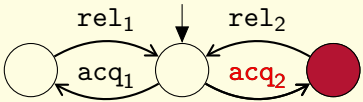

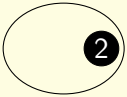

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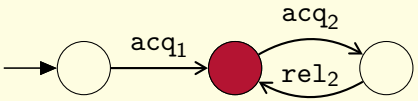

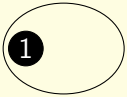

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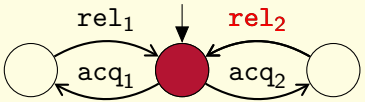

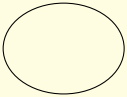

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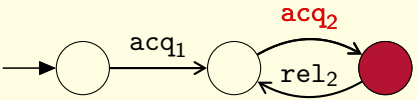

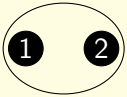

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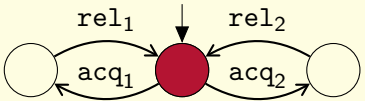

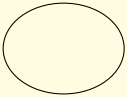

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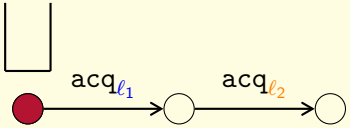
Restriction: Nested locking

All processes acquire and release locks in a **stack-like order**, i.e., a process can only release the lock it acquired the latest.



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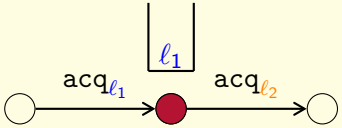

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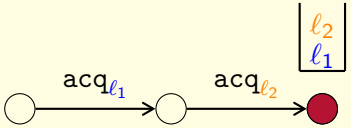

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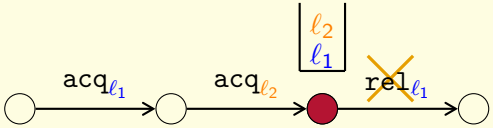

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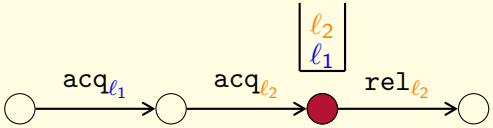

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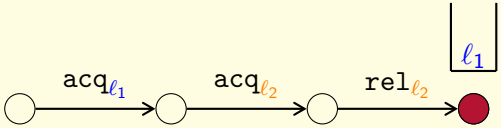

This restricts communication between processes.

Dynamic LSS

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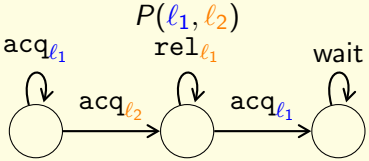
▷ A process can spawn other processes

▷ A process takes parameters, represented by *lock variables*

$Proc = \{P(\ell_1, \ell_2), Q(\ell_1, \ell_2, \ell_3), R(), ...\}$

Dynamic LSS[2]

Locks : 



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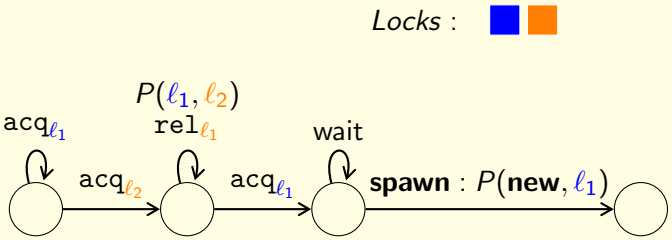

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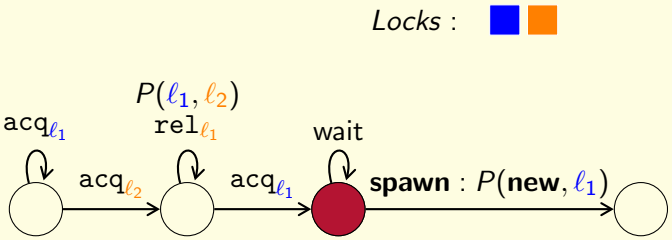

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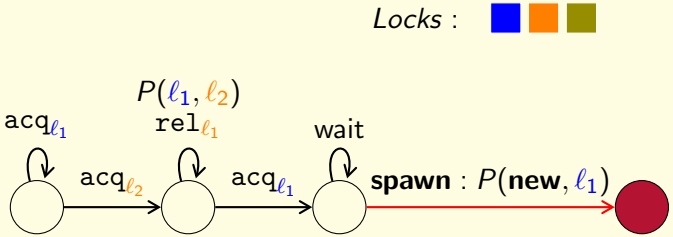

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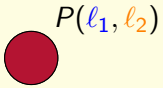
Tree representation



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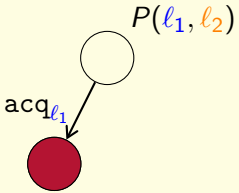

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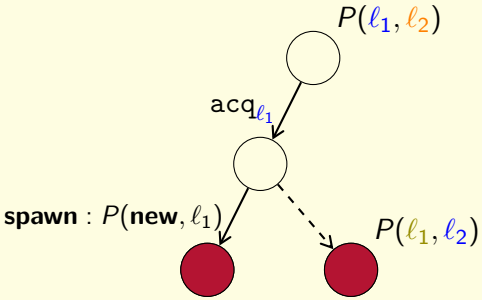

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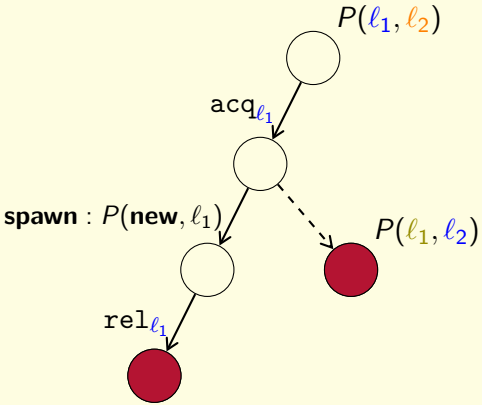

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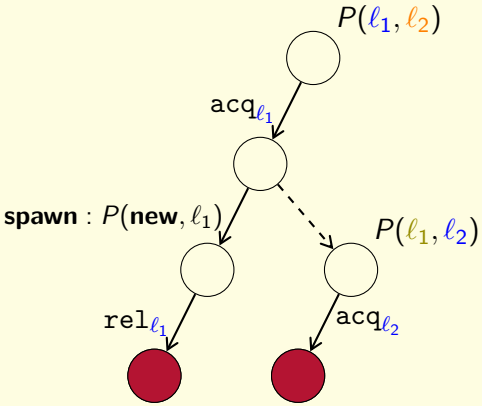

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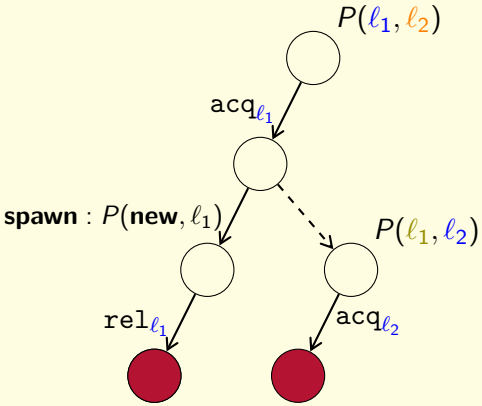

Specifications are ω-regular tree languages.

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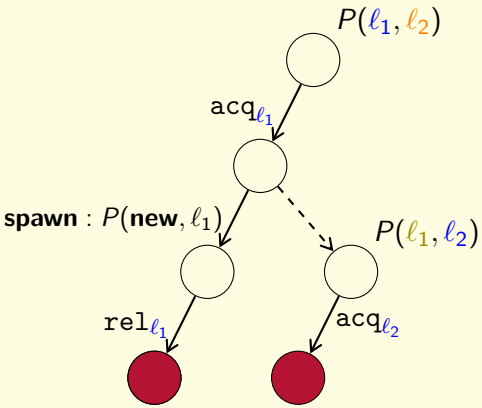

Specifications are ω-regular tree languages.

"Every process is blocked after some point"

"Finitely many processes are spawned"

"Infinitely many processes reach an error state q_{err}"

Deadlocks

Regular model-checking problem

Input: A DLSS $\mathcal{D}$ and a parity tree automaton $\mathcal{A}$.
Output: Is there a run of $\mathcal{D}$ accepted by $\mathcal{A}$?

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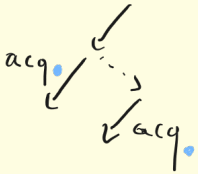

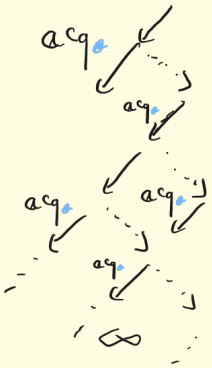

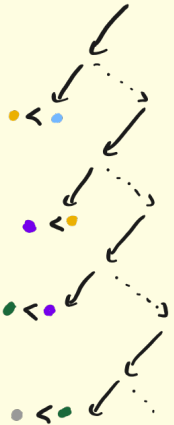

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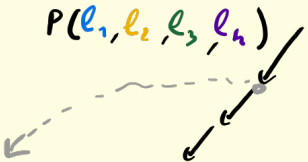
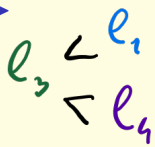


For each node we guess a label of the form

- "ℓ_1 is taken and will never be released", "ℓ_2 will be acquired infinitely many times", ...
- 

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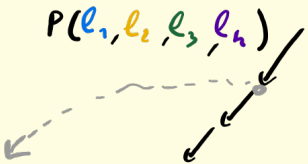

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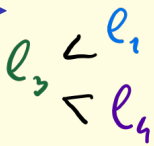
- 

The automaton checks that:

- the labels are consistent
- There exists a well-founded linear ordering on locks in which all local orders embed. (Technical part, also see related work [Demri Quaas, Concur '23])

Theorem [M., Muscholl, Walukiewicz Concur 2023]

Regular model-checking of DLSS is EXPTIME-complete, and
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What about pushdown processes?

Right-resetting pushdown tree automata

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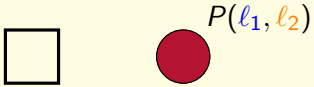
What about shared variables?

DLSS with variables



We add a register and operations `wr` and `rd` writing and reading letters from a finite alphabet in the register.

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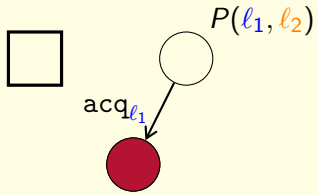

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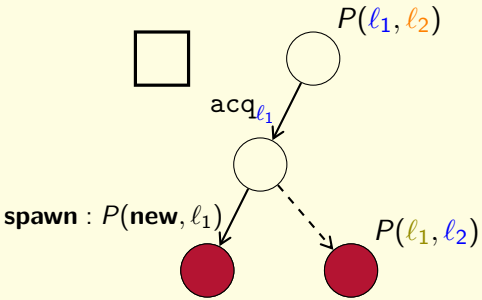

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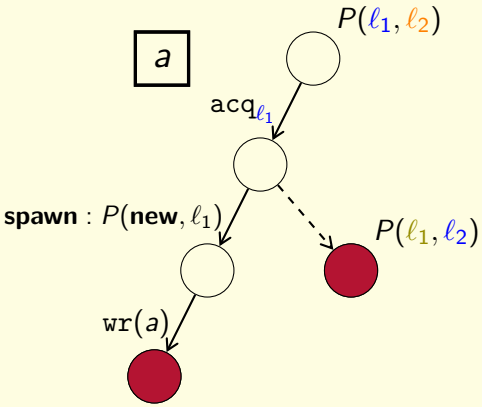

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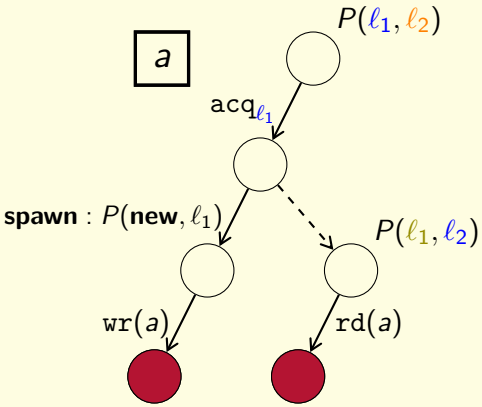

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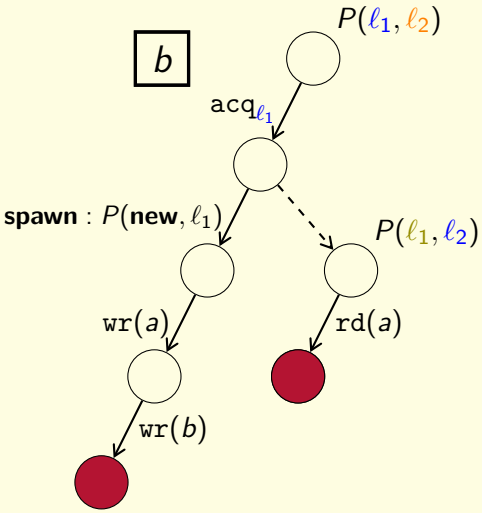

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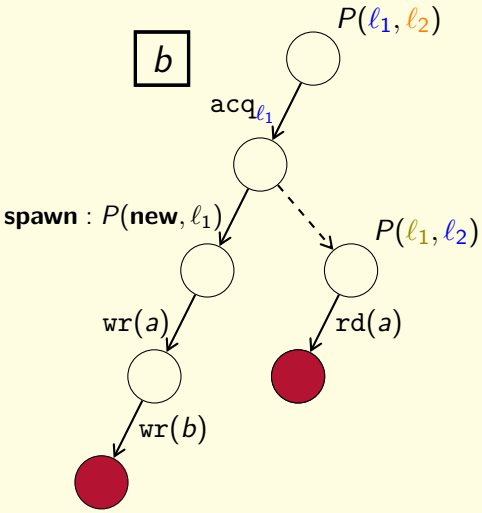

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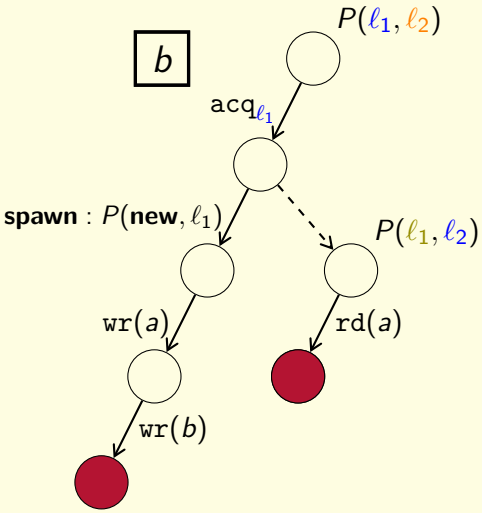

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Theorem

State reachability is undecidable for DLSS with variables.

Bounded writer reversals

Writer reversal = the process writing in the shared register changes.

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It is undecidable when the processes are pushdown systems[3].

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Lemma

Every finite run with a single writer can be cut into $2^{O(|Q|)}$ phases.

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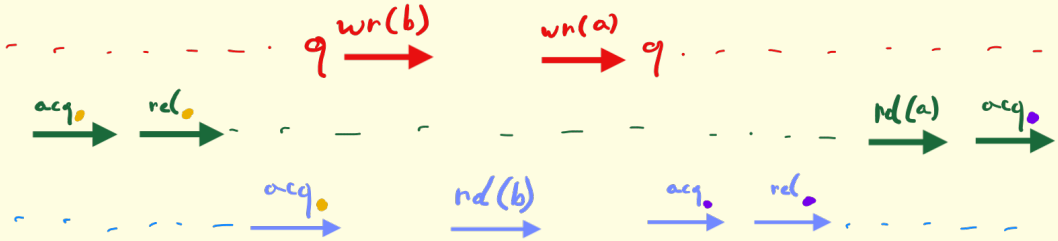
Every phase can be replaced by a sequence of phases where at most one reader moves.



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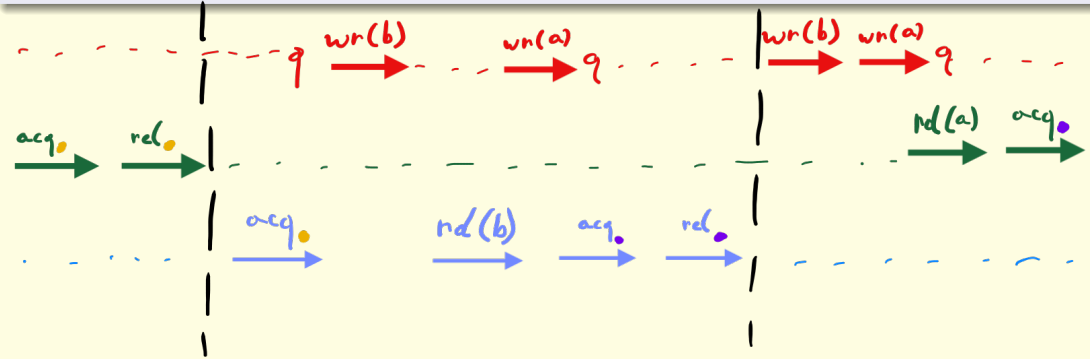

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Thanks!